Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits

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Speaker – Hao Chen

- I am a Ph.D. student in electrical and computer engineering at The University of Texas at Austin.

- I received the B.S. degree in electrical engineering from National Taiwan University (NTU) in 2019.

- Research interests: VLSI physical design and analog/mixed-signal circuit layout synthesis.
High Demand of Analog/Mixed-Signal IC

- Internet of Things (IoT), autonomous and electric vehicles, communication and 5G networks…

- Every sensor-related application needs analog circuits!!

Sources: IBM
Challenges of Analog Layout Routing

Human experience

Company A
Rules A

Company Z
Rules Z

Heuristic constraints

No comprehensive and exact descriptiveness!!

Aesthetic engineering

Hey, that looks strange, right?

Courtesy of [Ou+, TCAD’14]

Courtesy of [Rutenbar, TCACE’16]
Typical Automatic Analog Circuit Design Flow

Optimization-based approach

Schematic Design
- Circuit Spec.
  - Architecture & Topology Selection
  - Analog Sizing
    - Spec. Met?
      - N
      - Y
        - Analog Placement
        - Analog Routing
        - Spec. Met?
          - N
          - Y
            - Layout

Layout Design
- Placement
  - Routing
  - Constraints
- Final layout

Goal: Tape-out ready layout

- DRC/LVS clean
- Optimized performance
Analog Routing Constraints

- Symmetry constraints are widely accepted

Symmetry constraints

- Mirror symmetry
- Mirror self-symmetry

Routing Guide

Cannot be totally symmetric!!

[Xiao+, ICCAD’10][Ou+, TCAD’14][Zhu+, ICCAD’19]…
Analog Routing Constraints

• Symmetry constraints are widely accepted
Analog Routing Constraints

Symmetry constraints
- Mirror symmetry
- Mirror self-symmetry
- Cross symmetry
- Partial symmetry

New proposed constraints

Current matching, balancing

Electrical constraints
- Metal width lower bound for long wires
- Minimum number of cuts
- Avoid IR drop issues

- 2x2 cuts
- 1x2 cuts
- \( \geq W_1 \)
- \( \geq W_2 \)
Our AMS Routing Framework

- Repeat the routing process for each node in the hierarchy tree
Symmetry Constraint Allocation

- Assign symmetry constraints to nets according to pins locations
- Maximize the overall potential routing symmetry (Weighted graph matching)

\[
\text{Score} = \frac{\text{matched pins}}{\text{total pins}} = \frac{2}{5}
\]
Symmetry Constraint Allocation

• Assign symmetry constraints to nets according to pins locations

• Maximize the overall potential routing symmetry (Weighted graph matching)

\[
\text{Score} = \frac{\text{#matched pins}}{\text{#total pins}} = \frac{4}{5}
\]

Best axis

Net1

Net2

Net3

Net4
Symmetry Constraint Allocation

• Assign symmetry constraints to nets according to pins locations

• Maximize the overall potential routing symmetry (Weighted graph matching)
Symmetry Constraint Allocation

- Assign symmetry constraints to nets according to pins locations
- Maximize the overall potential routing symmetry (Weighted graph matching)

\[
\text{Score} = 2 \cdot \frac{\max(|N_2|, |N_3|)}{\max(|N_2|, |N_3|)} = 0
\]

\[|M_i| = \#\text{matched pins in net } i\]
Symmetry Constraint Allocation

- Assign symmetry constraints to nets according to pins locations
- Maximize the overall potential routing symmetry (Weighted graph matching)

\[
\text{Score} = 2 \cdot \frac{\max(|N_2|,|N_3|)}{\max(|N_2|,|N_3|)} = 2 \cdot \frac{2}{3} = \frac{4}{3}
\]

\[|M_i| = \#\text{matched pins in net } i\]
Symmetry Constraint Allocation

• Assign symmetry constraints to nets according to pins locations

• Maximize the overall potential routing symmetry (Weighted graph matching)

Sparse graph

Edmond’s blossom algorithm
Symmetry Constraint Allocation

• Assign symmetry constraints to nets according to pins locations

• Maximize the overall potential routing symmetry (Weighted graph matching)

Assigned Constraints

• Net1: self-symmetry

• Net2, Net3: symmetry

• Net4: self-symmetry
Pin Access Assignment

Design rule violations

Invalid points
Pin Clustering

$p_{i,j}$: the $j^{th}$ pin of net $i$

- Find the maximum subset of totally symmetric pins and form clusters
- Connect the pins in each cluster
- Connect the clusters and the remaining pins
Post Processing

Metal patching for design rules

patch metal

concave jog

clockwise

counterclockwise

convex jog

< w
Experimental Results

Setup
• C++ with Boost, Lemon
• CPU: Intel i9-7900X @ 3.3GHz

Benchmark circuits
• COMP: comparator
• OTA1: Miller compensation OTA
• OTA2: 2-stage feedforward compensation OTA
• ADC1: 2nd-order CT ΔΣ modulator
• ADC2: 3rd-order CT ΔΣ modulator

Benchmark

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>WL</th>
<th>VIA</th>
<th>Sym Deg.</th>
<th>DRV</th>
<th>Runtime (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMP</td>
<td>145.67</td>
<td>90</td>
<td>0.37</td>
<td>83</td>
<td>1.34</td>
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<tr>
<td>OTA1</td>
<td>520.64</td>
<td>167</td>
<td>0.31</td>
<td>170</td>
<td>36.30</td>
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<tr>
<td>OTA2</td>
<td>546.88</td>
<td>191</td>
<td>0.19</td>
<td>130</td>
<td>15.18</td>
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<tr>
<td>ADC1</td>
<td>2898.84</td>
<td>498</td>
<td>0.37</td>
<td>550</td>
<td>39.65</td>
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<tr>
<td>ADC2</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>Norm.</td>
<td>1.13</td>
<td>3.60</td>
<td>0.40</td>
<td>-</td>
<td>24.75</td>
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</tbody>
</table>

This work

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</thead>
<tbody>
<tr>
<td>COMP</td>
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<td>0</td>
<td>1.71</td>
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<tr>
<td>OTA2</td>
<td>523.40</td>
<td>79</td>
<td>0.70</td>
<td>0</td>
<td>0.37</td>
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<tr>
<td>ADC1</td>
<td>2686.60</td>
<td>175</td>
<td>0.62</td>
<td>0</td>
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<td>ADC2</td>
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<td>184</td>
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<td>18.82</td>
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<tr>
<td>Norm.</td>
<td>1.00</td>
<td>1.00</td>
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<td>-</td>
<td>1.00</td>
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13% WL reduction
DRC clean
24X speedup
Experimental Results

Setup
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Benchmark circuits
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- ADC1: 2nd-order CT ΔΣ modulator
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<th>[Zhu+, ICCAD'19]</th>
<th>This work</th>
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<tbody>
<tr>
<td>Fs (MHz)</td>
<td></td>
<td>320</td>
<td></td>
</tr>
<tr>
<td>BW (MHz)</td>
<td></td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>67.7</td>
<td>63.0</td>
<td>63.5</td>
</tr>
<tr>
<td>SFDR (dB)</td>
<td>84.8</td>
<td>78.0</td>
<td>81.7</td>
</tr>
<tr>
<td>Power (uW)</td>
<td>838.1</td>
<td>842.6</td>
<td>858.0</td>
</tr>
</tbody>
</table>

ADC1 simulation result

<table>
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<td>Power (uW)</td>
<td>838.1</td>
<td>842.6</td>
<td>858.0</td>
</tr>
</tbody>
</table>

OTA2 simulation result

<table>
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<th>Metrics</th>
<th>Schematic</th>
<th>[Zhu+, ICCAD'19]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
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<td>DC Gain (dB)</td>
<td>54.0</td>
<td>52.9</td>
<td>54.1</td>
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<tr>
<td>BW (MHz)</td>
<td>605.2</td>
<td>444.8</td>
<td>477.0</td>
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<tr>
<td>PM (degree)</td>
<td>64.1</td>
<td>75.3</td>
<td>76.1</td>
</tr>
<tr>
<td>Offset (uV)</td>
<td>-</td>
<td>893.3</td>
<td>145.7</td>
</tr>
<tr>
<td>Noise (uVrms)</td>
<td>12070.1</td>
<td>9711.5</td>
<td>9822.1</td>
</tr>
<tr>
<td>Power (uW)</td>
<td>428.7</td>
<td>424.3</td>
<td>439.7</td>
</tr>
</tbody>
</table>
## Experimental Results (ADC2)

### Monte-Carlo simulation

- **SNDR (dB)**
  - $\mu = 65.8$, $\sigma = 1.1$

- **SFDR (dB)**
  - $\mu = 76.0$, $\sigma = 3.5$

- **Power (uW)**
  - $\mu = 759.3$, $\sigma = 2.6$

### PVT simulation

<table>
<thead>
<tr>
<th>Corner</th>
<th>SNDR (dB)</th>
<th>SFDR (dB)</th>
<th>Power (uW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TT-N</td>
<td>66.1</td>
<td>79.8</td>
<td>759.0</td>
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<tr>
<td>TT-C</td>
<td>67.4</td>
<td>80.8</td>
<td>747.8</td>
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<tr>
<td>TT-H</td>
<td>64.3</td>
<td>78.3</td>
<td>774.7</td>
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<tr>
<td>FF-C</td>
<td>71.9</td>
<td>83.5</td>
<td>812.2</td>
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<tr>
<td>FF-H</td>
<td>65.4</td>
<td>82.7</td>
<td>854.4</td>
</tr>
<tr>
<td>SS-C</td>
<td>62.4</td>
<td>77.8</td>
<td>679.8</td>
</tr>
<tr>
<td>SS-H</td>
<td>62.1</td>
<td>76.8</td>
<td>711.9</td>
</tr>
</tbody>
</table>
Experimental Results (ADC2)

Taped-out and in measurements!!
Conclusions

AMS Router

• Symmetry constraint allocation
• Pin Access Assignment
• Hierarchical routing scheme for large/complicated systems with pin clustering
• Sign-off quality layout (DRC/LVS clean, performance guaranteed)

Future directions

• Advanced technology nodes (FinFET)
• Extended circuit classes
• This work is part of the MAGICAL project

• End-to-end analog layout automation system

• Open source at Github: https://github.com/magical-eda/MAGICAL
Thank you!