Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow

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This work is supported in part by the NSF under Grant No. 1704758, and the DARPA ERI IDEA program
Speaker – Keren Zhu

• Keren Zhu is a Ph.D. student at ECE Department at UT Austin under supervision of Prof. David Z. Pan.
• Keren Zhu’s research interests include general topics in VLSI physical design with a focus on analog layout automation.
Background: Automating AMS Layouts

- There are high demand for analog and mixed signal (AMS) circuits
- Drawing AMS layouts are still manual and cost time
Background: MAGICAL

- This work is part of MAGICAL
- Machine Generated Analog IC Layout

[GitHub Repository: https://github.com/magical-eda/MAGICAL]

**Placer codes**

**Benchmark netlists** (sanitized)
Motivation: placer v1

Placer v1. [Xu+ ISPD19]

- First version of MAGICAL placer prototype
- Abstracted problem formulation
- Not really consider performance yet
- NLP+LP

B. Xu, S. Li, C.-W. Pui, D. Liu, L. Shen, Y. Lin, N. Sun and D. Z. Pan, "Device Layer-Aware Analytical Placement for Analog Circuits," ISPD'19
Motivation: router v1

Placer v1. [Xu+ ISPD19]

Router v1. [Zhu+ ICCAD20]

• First version of MAGICAL router
• LVS correct
• Start working on optimizing performance with simulation results
• OTA/Comparator benchmarks

Motivation: hierarchical flow

Placer v1. [Xu+ ISPD19]

Router v1. [Zhu+ ICCAD19]

Hierarchical flow [Liu+ DAC20]

- MAGICAL start working on ADC
- Automatically tuning parameters for building block-level performance
- Manual tuning on top-level placement

Problem 1: system signal flow

- Manual tuned in DAC20

Diagram showing signal flow with different signal types: forward and feedback.

Optimized signal flow vs. Irregular signal flow (Default parameters).
Problem 2: sensitive building block performance

- Placer is not robust
  - Sensitive to the initial condition and parameters
  - Good results need some luck
  - Numerical optimization need to be improved

- IR drop is an issue
  - Placer should consider more in planning power routing
Motivation: placer v2

Placer v1 [Xu+ ISPD19]

Router v1 [Zhu+ ICCAD19]

Hierarchical flow [Liu+ DAC20]

Placer v2 [Zhu+ ICCAD20]
This work
Motivation: router v2

Placer v1 [Xu+ ISPD19]
Router v1 [Zhu+ ICCAD19]
Hierarchical flow [Liu+ DAC20]

This work

Placer v2 [Zhu+ ICCAD20]

Router v2 [Chen+ ICCAD20]
2A.3 Toward Silicon-Proven
Detailed Routing for Analog and Mixed-Signal Circuits
Motivation: router v2

Placer v1 [Xu+ ISPD19]
Router v1 [Zhu+ ICCAD19]
Hierarchical flow [Liu+ DAC20]

Placer v2 [Zhu+ ICCAD20]  
This work

Router v2 [Chen+ ICCAD20]

2A.3 Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits
Magical placer v2 has:

- New Power Net WL model
- New System Signal Flow Cost
- Self-adaptive multiplier updates
- Gradient-based NLP optimization

Building Block Level

System Level
Placer v2 flow

- Global placement decides the rough locations of each blocks
  - Iterative numerically solve non-linear optimization problem
  - Increase penalty multipliers for overlapping, etc. in each iteration
- Legalization ensure spacing and symmetry
  - Constraint graph + Linear programming

Placement Framework

- Global Placement
  - Init. Random Placement
  - Init. NLP Problem
  - Non-linear Optimization
  - Update NLP Problem

- Legalization
  - Area-driven Compaction
  - Wirelength-driven Compaction
System signal flow cost formulation

Want straight signal flow
System signal flow cost formulation

Minimize the angle $\theta$

$$1 - \cos(\theta) = 1 - \frac{\vec{v}_{i,j} \cdot \vec{v}_{j,k}}{\|\vec{v}_{i,j}\| \cdot \|\vec{v}_{j,k}\|},$$

$$\vec{v}_{i,j} = \begin{pmatrix} x_j - x_i \\ y_j - y_i \end{pmatrix}.$$
Fit more accurate power WL model

Disclaimer: this WL model is targeting for MAGICAL router v2

Pin-to-stripe power routing

\[ O_i^{\text{CRF}} = \sum_{k=1}^{\lfloor P_i^{\text{CRF}} \rfloor - 1} \max(y_i^{*,k+1} - y_i^{*,k}, 0), \]
Better multiplier updating scheme

- For better numerical robustness
- Matching initial gradient norm
  - Encourage comparable efforts to different costs

\[
\lambda^{(0)} = \min \left( \frac{\| \nabla f^{SWL(0)} \|}{\| \nabla f / \Phi^{(0)} \|}, \lambda_{MAX} \right),
\]

- Subgradient method to increase penalty

\[
\lambda^{(t)} = \lambda^{(t-1)} + \eta \cdot \Phi^{(t)}
\]

Use WL as common reference

Increase penalty based on how much is the violations
Gradient-based optimization

Algorithm 2 Optimization Kernel

1: $m_0 \leftarrow 0$
2: $v_0 \leftarrow 0$
3: $t \leftarrow 0$
4: while $(x, y)$ not converged do
5:     $t \leftarrow t + 1$
6:     if $t \leq t_{GD}$ then
7:         $g_t \leftarrow \nabla f(x, y)$
8:         $m_t \leftarrow \beta_1 \cdot m_{t-1} + (1 - \beta_1) \cdot g_t$
9:         $v_t \leftarrow \beta_2 \cdot v_{t-1} + (1 - \beta_2) \cdot g_t^2$
10:        $\hat{m}_t \leftarrow m_t / (1 - \beta_1^t)$
11:        $\hat{v}_t \leftarrow v_t / (1 - \beta_2^t)$
12:        $(x, y) \leftarrow (x, y) - \alpha \cdot \hat{m}_t / (\sqrt{\hat{v}_t + \epsilon})$
13:     else
14:        $(x, y) \leftarrow (x, y) - \delta \cdot \nabla f(x, y)$

Disclaimer: not well tuned. Adam with lower step size itself might also work.

How to update multipliers is in general more important than optimization kernels.

Adam optimizer for general cases.

Vanilla gradient descent when convergence is slow.
Legalization

- Generate a relational constraints and use linear programming to solve the compaction
- Similar to [Xu+ ISPD’19]
Experimental results on two ADCs

- System signal flow boosts the performance for two CTDSM ADCs

<table>
<thead>
<tr>
<th>Circuits</th>
<th>Schematic</th>
<th>Without SSF</th>
<th>With SSF</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ADC1</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>66.2</td>
<td>61.4</td>
<td>63.6</td>
</tr>
<tr>
<td>SFDR (dB)</td>
<td>76.9</td>
<td>75.0</td>
<td>77.1</td>
</tr>
<tr>
<td>THD (dB)</td>
<td>75.0</td>
<td>70.6</td>
<td>73.8</td>
</tr>
<tr>
<td>ENOB (bits)</td>
<td>10.70</td>
<td>9.90</td>
<td>10.27</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>0.837</td>
<td>0.864</td>
<td>0.870</td>
</tr>
<tr>
<td><strong>ADC2</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>67.1</td>
<td>59.6</td>
<td>66.3</td>
</tr>
<tr>
<td>SFDR (dB)</td>
<td>82.0</td>
<td>67.0</td>
<td>80.2</td>
</tr>
<tr>
<td>THD (dB)</td>
<td>77.6</td>
<td>66.5</td>
<td>76.4</td>
</tr>
<tr>
<td>ENOB (bits)</td>
<td>10.85</td>
<td>9.61</td>
<td>10.71</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>0.677</td>
<td>0.740</td>
<td>0.757</td>
</tr>
</tbody>
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Experimental results on block-level circuits

- Outperform [Xu+ ISPD19] in both WL and area

- More details in the paper

<table>
<thead>
<tr>
<th>CKTs</th>
<th>ISPD’ 19</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Area</td>
<td>HPWL</td>
</tr>
<tr>
<td>COMP</td>
<td>223</td>
<td>104</td>
</tr>
<tr>
<td>OP1</td>
<td>2366</td>
<td>767</td>
</tr>
<tr>
<td>OP2</td>
<td>2529</td>
<td>416</td>
</tr>
</tbody>
</table>
The ADC2 chip

- The ADC2 core using the proposed placer has been taped-out and verified in measurements.
Conclusion

- System signal flow is effective for two CTDSM-ADCs
  - Confirm with designers that this is a general approach for a broader range of circuit classes
- Better numerical optimization is effective in NLP global placement
- Fitting WL model to the target model is effective
  - Important for nets with special routing strategy

Future works:
- Placement and routing techniques for specific circuit classes
- Advance technology nodes
  - E.g. FinFET technology